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Swartz

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[54] **METHOD FOR FABRICATING A RADIATION HARDENED OXIDE HAVING TWO PORTIONS**

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[73] Assignee: **RCA Corporation**, Princeton, N.J.

[21] Appl. No.: **773,771**

[22] Filed: **Sep. 9, 1985**

[51] **Int. Cl.**[4] **H01L 21/473**; B05D 5/12

[52] **U.S. Cl.** **29/571**; 148/DIG. 118; 148/1.5; 427/93; 427/255.3

[58] **Field of Search** ..... 29/571, 576 B; 427/93, 427/255, 255.3, 255.4; 148/1.5, DIG. 118, DIG. 150, DIG. 116

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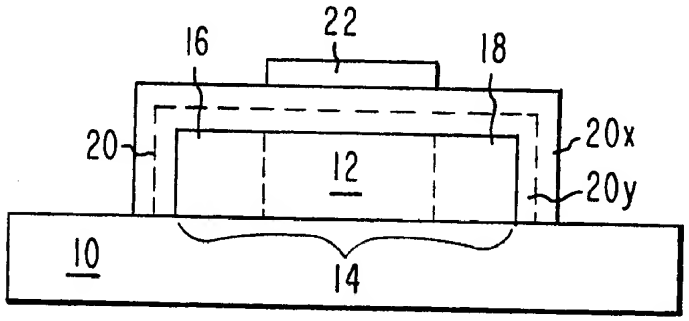
Primary Examiner—Olik Chaudhuri

Attorney, Agent, or Firm—Birgit E. Morris; William J. Burke; Henry I. Steckler

[57] **ABSTRACT**

A method for making a partially radiation hardened oxide comprises forming a first portion of an oxide layer on a semiconductor body of material at a temperature between about 950° C. and 1400° C., preferably between about 1000° C. and 1200° C. Thereafter a second portion of the oxide layer is formed between the semiconductor body and the first oxide layer at a temperature between about 850° C. and 900° C., preferably at about 875° C.

16 Claims, 6 Drawing Figures



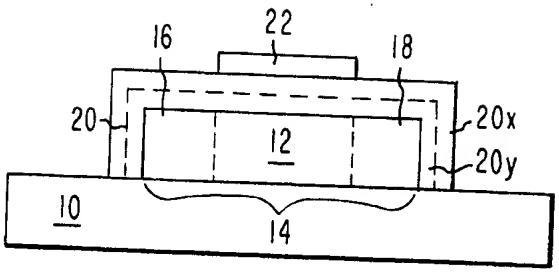


Fig. 1

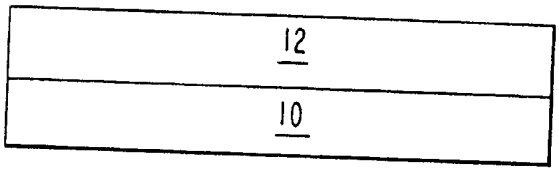


Fig. 2

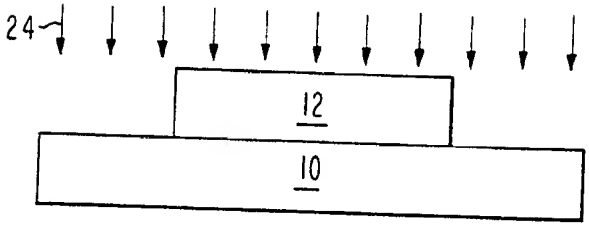


Fig. 3

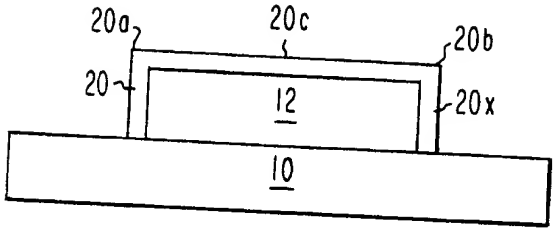


Fig. 4

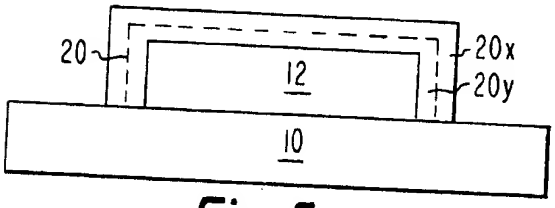


Fig. 5

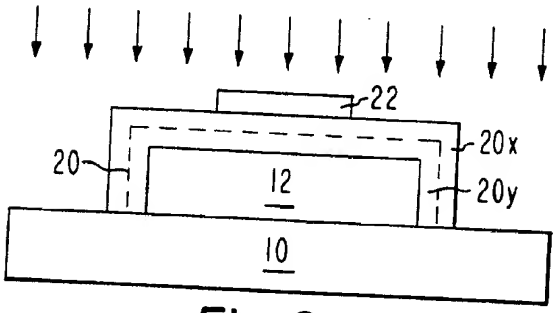


Fig. 6

METHOD FOR FABRICATING A RADIATION HARDENED OXIDE HAVING TWO PORTIONS

BACKGROUND OF THE INVENTION

The present invention relates to a method for making a radiation hardened oxide, and more particularly, to a method for making a radiation hardened device incorporating such an oxide located adjacent an edge.

It is known that a silicon-on-sapphire (SOS) metal oxide semiconductor field effect transistor (MOSFET) with a gate oxide insulating layer grown in a steam ambient at or below about 900° C. is at least partially radiation hard, i.e. changes in the gate threshold voltage are reduced after irradiation by gamma rays as compared to a MOSFET that is not radiation hardened. However, it has been found that oxides grown at these temperatures on a silicon mesa are thinner near the mesa edges than at the center thereof, thereby lowering the breakdown voltage and increasing the tunneling current of the oxide. Oxides grown at higher temperatures are more nearly of uniform thickness, see R. B. Marcus et al. "The Oxidation of Shaped Silicon Surfaces", J. Electrochemical Soc., Vol. 129, (June 1982), pages 1278 to 1282. This reduces the tunneling current and increases the breakdown voltage as compared to oxides grown at the lower temperatures for a given thickness at the mesa center, but such high temperature grown oxides are not radiation hard.

SUMMARY OF THE INVENTION

A method in accordance with the present invention comprises forming a first portion of an oxide layer on a body of material at a temperature between about 950° C. and 1400° C., preferably between about 1000° C. and 1200° C., and forming a second portion of said oxide layer between about 850° C. and 900° C., preferably at 875° C., said second portion being disposed adjacent said body.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a device made in accordance with the invention; and

FIGS. 2-6 are cross-sectional views of said device during sequential manufacturing steps.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 shows an insulating substrate 10, such as sapphire (Al_2O_3), having a mesa-shaped P−-type conductivity epitaxial silicon body of material 12 thereon. A device, such as a MOSFET 14, is disposed in the body 12 and has an N+-type conductivity source region 16, an N+-type conductivity drain region 18, a gate insulating layer 20, such as silicon dioxide (SiO_2), disposed on body 12, and a gate 22, such as polycrystalline silicon (polysilicon), disposed on layer 20. In accordance with the invention, layer 20 comprises an outer first portion 20*x* and an inner second portion 20*y*, said portions being formed at different temperatures, as explained in detail below.

FIG. 2 shows the starting material for making the device 14, namely the substrate 10 and the epitaxial body 12. By masking followed by reactive ion etching (RIE), the body 12 is formed into a mesa, as shown in FIG. 3. The body 12 is then lightly doped, such as by ion implantation with boron, as indicated by arrows 24.

As shown in FIG. 4 and in accordance with the invention, the first portion 20*x* of insulating layer 20 is grown in an oxygenating ambient, such as steam or dry oxygen (O_2), with the body 12 and the steam or dry O_2 at a temperature between about 950° C. and 1400° C. The lower temperature limit is about the minimum temperature at which the thickness at the corners 20*a* and 20*b* of the portion 20*x* is about the same as the thickness at the center 20*c* thereof, while the upper temperature limit is about the melting point of silicon. In practice, a lower limit of about 1000° C. is usually chosen to ensure that the portion 20*x* has a uniform thickness, while an upper limit of about 1100° C. is usually chosen if steam is the ambient and an upper limit of about 1200° C. is usually chosen if dry O_2 is the ambient, since above these temperatures the portion 20*x* forms too fast for accurate control of the thickness thereof.

Thereafter as shown in FIG. 5, the second portion 20*y* of layer 20 is formed by reducing the temperature of the body 12 and the ambient to between about 850° C. and 900° C., preferably at about 875° C. It has been found that at these temperatures oxidation in a steam ambient, but not in dry O_2, produces radiation hardening. Below about 850° C. forming portion 20*y* takes too long, while above about 900° C. the portion 20*y* is not radiation hard. During this forming step, the water molecules diffuse through the portion 20*x* to the layer 12 to form portion 20*y* disposed between layer 12 and portion 20*x*. Typically portions 20*y* and 20*x* have thicknesses which are about one-quarter and about three-quarters, respectively, of the total thickness of layer 20. It is believed that portion 20*y* should have a minimum thickness of about 10 nanometers (nm) for adequate radiation hardening. The result is that layer 20 is radiation hardened as compared to oxide layers grown above about 900° C. due to portion 20*y* being adjcent the silicon-SiO_2 interface where radiation hardening is required. Further, since most of the thickness of layer 20 is that of portion 20*x* of relatively uniform thickness, layer 20 also has relatively uniform thickness. Therefore, layer 20 has a relatively high breakdown voltage and relatively small tunneling current as compared with oxide layers entirely grown at between about 850° C. and 900° C. for the same value of thickness at the center 20*c*.

The remaining steps are conventional. In particular, a polysilicon layer is deposited and defined to form the gate 22 as shown in FIG. 6. Thereafter, an N-type conductivity dopant, such as phosphorous, is ion implanted as shown by arrows 28 to form the self-aligned source and drain regions 16 and 18, respectively, of FIG. 1, and to improve the conductivity of gate 22. The MOSFET 14 is then annealed to activate the implants at a temperature equal to or below the temperature at which portion 20*y* is formed. Then glass (not shown) is deposited and reflowed, contact openings (not shown) formed therein, and metallization applied to the source and drain regions 16 and 18, respectively.

While the above description is directed to an N-channel device, it will be appreciated that the method of the invention is equally applicable to a P-channel device wherein the layer 12 is of N−-type conductivity and source and drain regions 16 and 18, respectively, are of P-type conductivity that can be formed by boron ion implantation.

EXAMPLE NO. 1

Three groups of capacitors, i.e. the structure of FIG. 1, comprising substrate **10** (formed of bulk silicon for economic reasons), body **12**, layer **20**, and gate **22**, but without source and drain regions **16** and **18**, respectively, have been fabricated with a 70 nm thick layer of SiO_2. The first group had all of layer **20** grown at 1100° C., the second group had all of layer **20** grown at 900° C., and the third group had portion **20***x* grown at 1100° C. with a thickness of about 53 nm and portion **20***y* grown at 900° C. with a thickness of about 17 nm. Then the capacitors were irradiated. Thereafter the capacitors were tested by measurements of capacitance versus voltage for the inversion voltage thereof, which essentially corresponds to the threshold voltage of a MOSFET. The inversion voltage of capacitors from the second and third groups were essentially identical for radiation doses up to 1 Meg Rad. This shows that a layer **20** formed of two potions at a high and a low temperature respectively has the same amount of radiation hardness as a single temperature formed layer **20** when the single temperature is equal to the low temperature. The capacitors from the first group had inversion voltages four times greater than those from the second and third groups for radiation doses of from 300 Krads to 1 Meg Rad. Therefore the single higher temperature formed layer **20** had a lower amount of radiation hardness than either the single low temperature formed layer **20** or the two temperature formed layer **20**.

EXAMPLE NO. 2

Three groups of capacitors were fabricated identically to those described in Example No. 1 except that the thickness of layer **20** was about 60 nm, the second group had layer **20** formed at 875° C., and the third group had portion **20***y* formed at 875° C. with a thickness of about 15 nm. The breakdown voltage for the first, second, and third groups were 8.5 Megavolts (MV)/cm, 7 MV/cm, and 7.7 MV/cm, respectively. Thus the two temperature formed layer **20** has a breakdown voltage that is closer to the single low temperature formed layer **20**. Further, the tunneling current for the third group was about 500 times less than those of the second group. Therefore the two temperature formed layer **20** has a lower tunneling current than the single low temperature formed layer **20**.

The present invention is applicable not only to a MOSFET formed on SOS, but to any device formed adjacent an edge, e.g. a device, such as a capacitor, formed on a mesa, or a device having a groove, such as a vertical metal oxide semiconductor (VMOS), or any device having trench isolation.

What is claimed is:

1. A method for making a radiation hardened oxide layer comprising:

forming a first portion of said oxide layer on a body of silicon semiconductor material at a temperature of between about 950° C. and 1400° C.; and

forming a second portion of said oxide layer in a steam ambient at a temperature between about 850° C. and 900° C., said second portion being disposed between said body and said first portion.

2. The method of claim **1**, wherein said body has a temperature of between about 1000° C. and 1200° C. during said first recited forming step.

3. The method of claim **1**, wherein said second portion has a minimum thickness of about 10 nm.

4. The method of claim **1**, wherein said second recited forming step is performed at a temperature of about 875° C.

5. The method of claim **1**, wherein said body comprises a silicon mesa disposed on an insulating substrate and further comprising:

forming a gate on said oxide layer; and

forming source and drain regions in said mesa adjacent said gate.

6. The method of claim **5**, wherein said step of forming said gate comprises depositing and defining polycrystalline silicon.

7. The method of claim **5**, wherein said step of forming source and drain regions comprises ion implanting a conductivity modifying dopant.

8. The method of claim **1**, wherein said first portion has a thickness of about three times the thickness of said second portion.

9. A method for making a radiation hardened oxide layer comprising:

forming by thermal oxidation a first portion of said oxide layer on a silicon body at a temperature of between about 950° C. and 1400° C.; and

forming a second portion of said oxide layer in a steam ambient at a temperature between about 850° C. and 900° C., said second portion being disposed between said body and said first portion.

10. The method of claim **9**, wherein said body has a temperature of between about 1000° C. and 1200° C. during said first recited forming step.

11. The method of claim **9**, wherein said second portion has a minimum thickness of about 10 nm.

12. The method of claim **9**, wherein said second recited forming step is performed at a temperature of about 870° C.

13. The method of claim **9**, wherein said body comprises a mesa disposed on an insulating substrate and further comprising:

forming a gate on said oxide layer; and

forming source and drain regions in said mesa adjacent said gate.

14. The method of claim **13**, wherein said step of forming said gate comprises depositing and defining polycrystalline silicon.

15. The method of claim **13**, wherein said step of forming source and drain regions comprises ion implanting a conductivity modifying dopant.

16. The method of claim **9**, wherein said first portion has a thickness of about three times the thickness of said second portion.

* * * * *

US006281138B1

(12) **United States Patent**
Brady et al.

(10) **Patent No.: US 6,281,138 B1**
(45) **Date of Patent: Aug. 28, 2001**

(54) **SYSTEM AND METHOD FOR FORMING A UNIFORM THIN GATE OXIDE LAYER**

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(73) Assignee: **Agere Systems Guardian Corp.**, Orlando, FL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/338,939**

(22) Filed: **Jun. 24, 1999**

Related U.S. Application Data

(62) Division of application No. 08/848,109, filed on Apr. 28, 1997, now Pat. No. 6,025,280.

(51) **Int. Cl.**[7] **H01L 21/31**; H01L 29/04; H01L 29/76

(52) **U.S. Cl.** **438/762**; 438/770; 438/787; 438/790; 257/410; 257/57

(58) **Field of Search** 438/762, 770, 438/787, 790, 33, 37; 257/410, 57

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Primary Examiner—Olik Chaudhuri
Assistant Examiner—Shrinivas H. Kao

(57) **ABSTRACT**

This invention includes a novel synthesis of a three-step process of growing, depositing and growing SiO_2 under low pressure, e.g., 0.2–10 Torr, to generate high quality, robust and reliable gate oxides for sub 0.5 micron technologies. The first layer, 1.0–3.0 nm is thermally grown for passivation of the Si-semiconductor surface. The second deposited layer, which contains a substantial concentration of a hydrogen isotope, such as deuterium, forms an interface with the first grown layer. During the third step of the synthesis densification of the deposited oxide layers occurs with a simultaneous removal of the interface traps at the interface and growth of a stress-modulated SiO_2 occurs at the Si/first grown layer interface in the presence of a stress-accommodating interface layer resulting in a planar and stress-reduced Si/SiO_2 interface. The entire synthesis is done under low-pressure (e.g., 0.2–10 Torr) for slowing down the oxidation kinetics to achieve ultrathin sublayers and may be done in a single low-pressure furnace by clustering all three steps.

6 Claims, 1 Drawing Sheet

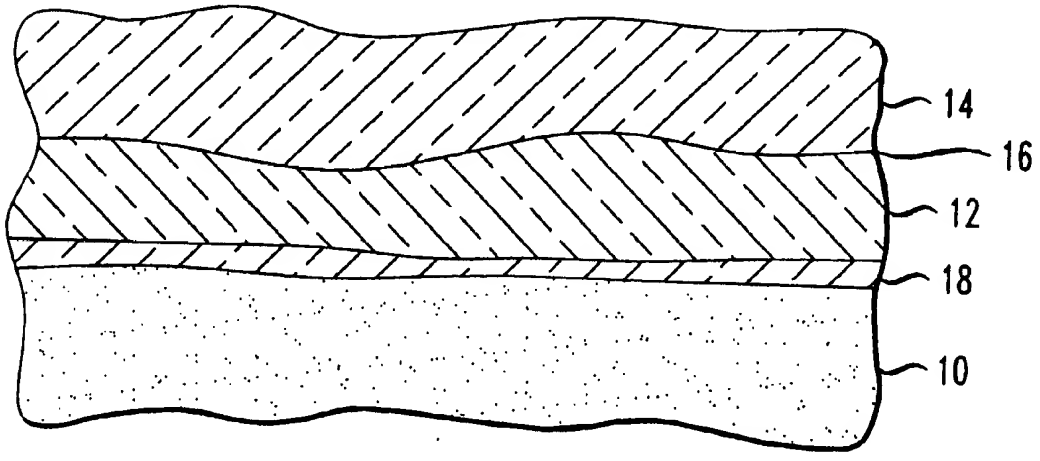


FIG. 1

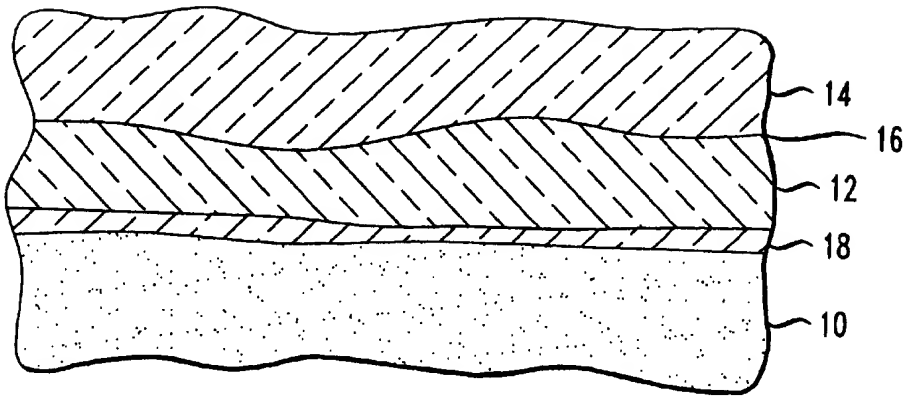
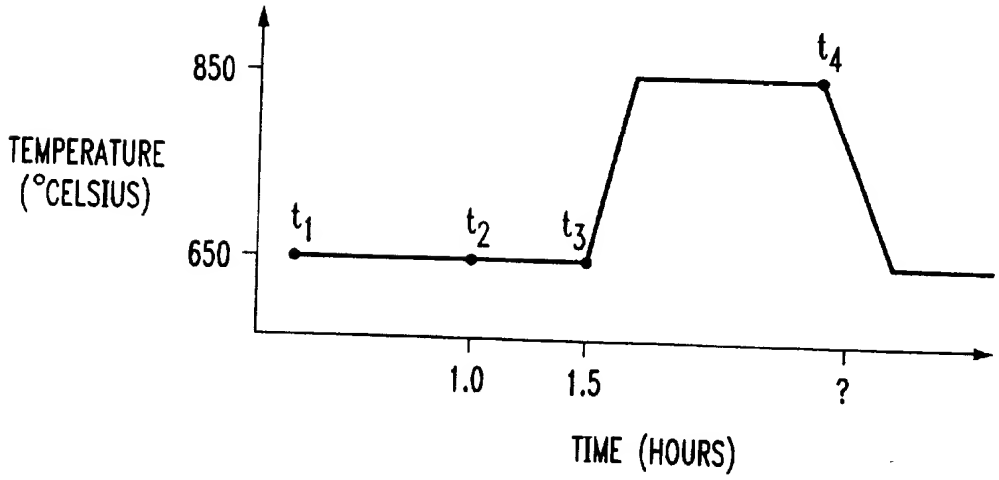

14
16
12
18
10

FIG. 2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(°CELSIUS)
t1
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1.0
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?
TIME (HOURS)

SYSTEM AND METHOD FOR FORMING A UNIFORM THIN GATE OXIDE LAYER

This application is a Divisional of prior application Ser. No. 08/848,109, filed Apr. 28, 1997, now U.S. Pat. No. 6,025,280 to David C. Brady, et al. The above-referenced Patent is commonly assigned with the present invention and is incorporated herein by reference as if reproduced herein in its entirety under Rule 1.53(b).

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to integrated circuit fabrication and, more specifically, to a system and method for forming a uniform, ultrathin gate oxide layer on a semiconductor substrate.

BACKGROUND OF THE INVENTION

As metal-oxide-semiconductor ("MOS") technology continues to advance and the features of the MOS devices shrink, a scaling down in the vertical dimension of the devices typically occurs. Critical to the success of these devices is a reliable, highquality gate-dielectric with a low defect density ("D_o") and a high breakdown field strength ("F_{bd}") that retains its quality during advanced processing. As the overall thickness of the gate dielectric gets ultrathin (e.g., less than 7.5 nm), the quality of the oxide (e.g., SiO_2), even under the best possible external growth conditions, is limited by the natural viscoelastic compressive stress generated in the SiO_2 at temperatures below 1000° C. and by the thermal expansion mismatch between silicon substrate and SiO_2. In present applications, a genuine lowering of the D_o in the range of 0.05 to 0.5 cm^{-2} has been achieved. For example, oxide/nitride or oxide/nitride/oxide (ONO) structures can attain such low D_o. The Si_3N_4—SiO_2 ("silicon nitride-silicon oxide") interface, however, is invariably associated with a high density of interface states ("Q_{it}") that cannot be annealed out easily because the Si_3N_4 layer is impervious to diffusion of oxidizing species. These multilayered dielectrics are unsuitable as gate dielectrics in advanced complementary metal-oxide-semiconductor ("CMOS") integrated circuits, because the interface states may cause charge-induced shift in the threshold voltage and can reduce the channel conductance during operation.

To overcome this problem, the concept of stacking thermally grown and chemical-vapor-deposited ("CVD") SiO_2 structures has been proposed in U.S. Pat. No. 4,851,370 ("the '370 patent"), which is incorporated herein by reference for all purposes. Here, the composite stack is synthesized by a 3-step grow-deposit-grow technique wherein the growing steps are conducted at pressures equal to or greater than one atmosphere. The interface between the grown and deposited SiO_2 layers serves the same purpose as the interface in SiO_2—Si_3N_4 structures (i.e., it reduces the D_o by misaligning the defects across the interface). Moreover, the interface traps in stacked oxide structures that can be removed easily by an oxidizing anneal, since the top deposited SiO_2 layer, unlike the Si_3N_4 film, is transparent to oxidizing species (i.e., it transports them by diffusion). This stacking concept can be applied to any composite dielectric structure with similar results as long as the top deposited dielectric layer is transparent to the oxidizing species.

A few major factors contributing to defects in conventional thin-oxide gate dielectrics are growth-induced micropores and intrinsic stress within the oxide layer. The micropores are 1.0 nm to 2.5 nm in diameter, with an average separation of about 10.0 nm. The pores form at

energetically favored sites such as heterogeneities created by localized contaminants, ion-damaged areas, dislocation pile-ups and other defect areas on the silicon surface resulting from retarded oxidation in these sites. The pores grow outward as oxidation continues to consume silicon around the pore. Thus, a network of micropores usually exists in SiO_2. The micropore network forms potential short-circuit paths for diffusional mass transport and for current leakage.

In addition, the stress within a SiO_2 layer, often accentuated by complex device geometries and processing, usually increases both the size and density of the micropores. Therefore, in developing thin dielectrics with ultra-low D_o, not only should the initial D_o be reduced, but also the local stress-gradients near the Si—SiO_2 interface should be reduced by providing a stress-accommodating layer, such as an interface (between grown and deposited layers) within the dielectric that acts as a stress cushion and defect sink.

The above-mentioned problems become even more acute as the overall size of devices decrease to sub-micron size with ultrathin gate dielectrics (e.g., less than 7.5 nm). Unfortunately, however, the above-discussed conventional stacked-oxide process, which works extremely well in technologies where the gate dielectric thickness is greater than 7.5 nm, is not as applicable in technologies having thicknesses less than 7.5 nm. The main reason for this is that in the conventional 3-step stacked process, the SiO_2 is grown in pressures of one atmosphere or greater. In semiconductor technologies where the gate oxide thickness is 10.0 nm or greater, this particular condition is most advantageous because under such atmospheric pressure, the SiO_2 can be grown quite rapidly and one can grow the first grown layer (typically 1.0–7.5 nm) with good uniformity. This rapid growth is highly desirable, for it cuts down in manufacturing time, and thus, overall production costs. This same rapid growth, which is so advantageous in technologies with gate oxide thickness of 10.0 nm or greater is less desirable in sub-0.5 micron semiconductor technologies because the oxides grow too quickly, which makes thicknesses harder to control. As such, the oxide layers are less uniform in thickness, which is unacceptable.

Furthermore, performance degradation of these devices that occurs with time, which is often referred to as the hot carrier (electron or hole) degradation effect, is also well known. It is believed that this efficiency degradation is caused by defects that are generated by the current flow through the device. It is believed that these defect states reduce the mobility and lifetime of the carriers and cause degradation of the device's performance. In most cases, the substrate comprises silicon, and the defects are thought to be caused by dangling bonds (i.e., unsaturated silicon bonds) that introduce states in the energy gap, which remove charge carriers or add unwanted charge carriers in the device, depending in part on the applied bias. While dangling bonds occur primarily at surfaces or interfaces in the device, they also are thought to occur at vacancies, micropores, dislocations, and are also thought to be associated with impurities. To alleviate the problems caused by such dangling bonds, a hydrogen passivation process has been adopted and has become a well-known and established practice in the fabrication of such devices.

In the hydrogen passivation process, it is thought that the defects that affect the operation of semiconductor devices are removed when the hydrogen bonds with the silicon at the dangling bond sites. While the hydrogen passivation process eliminates the immediate problem associated with these dangling bonds, it does not eliminate degradation permanently because the hydrogen atoms that are added by the

passivation process can be "desorbed" or removed from the previous dangling bond sites by radiation or by the "hot carrier effect."

A hot carrier is an electron or hole that has a high kinetic energy that is imparted to it when voltages are applied to the electrodes of the device. Under such operating conditions, the hydrogen atoms, which were added by the hydrogen passivation process, are knocked off by the hot electrons, and result in aging or degradation of the device's performance. According to established theory, this aging process occurs as the result of hot carriers stimulating the desorption of hydrogen from the silicon substrate's surface or SiO_2 interface. This hot carrier effect is particularly of concern with respect to smaller devices.

Accordingly, what is needed in the art is a stacked-oxide process that provides gate dielectrics having thickness than 10.0 nm and, more advantageously less than 7.5 nm, and yet provides a semiconductor that has a low defect density ("D_d") and a high breakdown field strength ("F_{bd}") that retains its quality during advanced processing. The present invention addresses this need.

SUMMARY OF THE INVENTION

To address the above-discussed deficiencies of the prior art, the present invention provides a semiconductor and systems and methods of manufacture thereof. One method includes the following grow-deposit-grow steps: (1) growing a first oxide layer on the semiconductor substrate in a zone of low pressure, (2) depositing a dielectric layer on the first oxide layer in the zone of low pressure, wherein the dielectric layer has a substantial concentration of a hydrogen isotope therein and (4)growing a second oxide layer between the first oxide layer and the substrate in the zone of low pressure. The zone of low pressure is created to retard the oxidation rate at which the first and second oxide layers are grown.

The present invention therefore introduces the broad concept of growing the first and second oxide layers under low pressure oxidizing conditions to retard their growth. Such retardation of the growth rate is necessary given the thinness and uniformity desired in the dielectric sub-layers in sub-micron technologies. Additionally, the present invention also presents a deposited layer that has a substantial concentration of a hydrogen isotope, such as deuterium incorporated therein. For purposes of the present invention, "substantial concentration" is defined as a concentration of at least 10^{16} cm^{-3} of the isotope of hydrogen relative to nonisotopic hydrogen. It is believed that the additional mass allows the deposited layer to be deposited in a slower and more controlled manner, thereby providing a more uniform deposited layer. When this advantage is combined with the other advantages obtained from growing the oxides under low pressure, a semiconductor device having a uniformity and robustness that are superior to those found in the prior art is provided.

In one embodiment of the present invention, the second grown oxide layer may have a thickness of less than 10 nm or between about 0.5 nm and about 0.8 nm and may be grown at a temperature exceeding 800° C.

In one embodiment of the present invention, the steps of growing, depositing and growing are performed in a single vapor deposition apparatus. That the method of the present invention may be performed in a single "tool" or "furnace" allows high rates of production and greater process control, although, performance in a single tool is not required.

In one embodiment of the present invention, a pressure in the zone of low pressure ranges from about 200 milliTorr to about 950 milliTorr. In a more specific embodiment, the pressure is about 900 milliTorr during the step of growing the first and second oxide layers and about 400 milliTorr during the second step of depositing the dielectric layer.

In one embodiment of the present invention, a thickness of the first grown oxide layer is less than about 5.0 nm. In a more specific embodiment of the present invention, however, the thickness is about 1.0 nm.

In another embodiment of the present invention, the deposited dielectric layer is generated from the decomposition of a deuterated tetraethyl orthosilicate ("TEOS") or a deuterated silane (SiD_4) and has a thickness of about 1.5 nm. In a more specific embodiment of the present invention, the thickness ranges from about 1 nm to about 4.0 nm. The TEOS is preferably deposited at a flow rate of 50 cubic centimeters per minute.

In one embodiment of the present invention, the steps of growing and depositing are performed at a temperature that ranges from about 600° C. to about 750° C. In yet another embodiment, the step of growing the second oxide layer is performed at a temperature ranging from about 800° C. to about 1000° C.

In one embodiment of the present invention, the step of growing the first oxide layer is performed under a pressure of 900 milliTorr and the oxygen has a flow rate of 9 standard liters per minute. In yet another embodiment, the step of growing is performed under a nitrous oxide and nitrogen environment wherein the nitrous oxide has a flow rate of about 1.72 standard liters per minute and the nitrogen has a flow rate of about 0.75 standard liters per minute to attain light-nitridation, (1–5%) near the interface between the first and second grown oxide layers.

In another aspect of the present invention, a semiconductor comprising of a substrate and having a stress-accommodating layer formed therein is provided. The gate dielectric has a thickness less than 7.5 nm and comprises: (1) a first grown oxide layer on the substrate that was formed on an exposed surface of the substrate in a zone of low pressure, (2) a deposited dielectric layer having a substantial concentration of a hydrogen isotope incorporated therein and formed over the first grown oxide layer in the zone of low pressure and (3) a second grown oxide layer formed between the first oxide layer and the substrate that was formed in the zone of low pressure. The zone of low pressure is created to retard a rate at which the first and second oxide layers are grown. During this third-step of stacked oxide synthesis oxide growth occurs under a stress-modulating condition provided by the interface between the first grown and second deposited layer generating a planar and stress-free substrate Si/SiO_2 interface which can otherwise never be achieved by conventional 1-step oxide growth.

In one embodiment of this aspect of the present invention, the first grown oxide, the second deposited dielectric and the second grown oxide layers are formed on the substrate in a single low-pressure vapor deposition apparatus. As previously stated, this offers the advantage of decrease production cycle time and thus production cost.

In one embodiment of this aspect of the present invention, the second grown oxide layer may be formed at a temperature exceeding about 800° C., and the first oxide layer and the dielectric layer may be grown in a temperature exceeding about 600° C. The second grown oxide layer may have thickness that ranges from about 0.5 nm to about 0.8 nm.

In one embodiment of this aspect of the present invention, the deposited dielectric layer is formed in a pressure of about 400 milliTorr in the zone of low pressure and may have a

thickness of about 1.5 nm. In yet another aspect of this particular embodiment, the deposited dielectric layer is formed from the decomposition of TEOS, which preferably had a flow rate of 50 cubic centimeters per minute during its deposition.

In one embodiment of this aspect of the present invention, the first oxide layer may have a thickness of less than about 5.0 nm (preferably in the range of 1.0 nm to 3.0 nm).

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention that are described hereinafter form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates a schematic representation of a structure according to an advantageous embodiment of the present invention; and

FIG. 2 illustrates a schematic graph of the thermal, pressure and flow rate history for an oxidation scheme in accordance with an advantageous embodiment of the present invention.

DETAILED DESCRIPTION

Referring initially to FIG. 1, there is illustrated a schematic representation of a structure according to an advantageous embodiment of the present invention. In one such embodiment, a substrate **10** is used, and a 1 nm to 2.5 nm oxide layer **12** is formed on the substrate under a low pressure, for example, a pressure of less than 10 Torr. In more advantageous embodiments, the pressures are at less than about 2 Torr. In one advantageous embodiment, the substrate **10** may be silicon and the oxide layer **12** may be silicon dioxide (SiO_2) that is thermally grown from the substrate **10** to a thickness that may range from about 1 nm to about 2.5 nm. However, it will be appreciated by those skilled in the art that other materials presently used in the manufacturer of semiconductor devices may be used or materials later-determined to be useful for such manufacture may also be used. Moreover, it is within the scope of the present invention that the oxide layer **12** could also be deposited, as long as it has a different defect structure compared to the second deposited layer. However, as just mentioned above, it is desirable that the oxide layer **12** be thermally grown.

Depending on the particular embodiment, the low pressure under which the oxide layer **12** is grown may range from about 0.4 Torr to about 10 Torr and the temperature may range from about 350° C. to about 1000° C. In one embodiment, the oxygen flow may be at a rate that ranges from about 5 standard liters per minute (slm) to about 25 slm. However, in an advantageous embodiment, the pressure under which the oxide layer **12** is grown under a pressure of about 900 milliTorr and the temperature may range from about 600° C. to about 750° C.

Forming the oxide layer **12** under low pressure is a radical departure from the conventional stacked oxide synthesis, in which the oxide layer is grown under a pressure of one atmosphere or greater. In conventional stacked oxides, pressures of one atmosphere or greater were necessary to grow the first oxide layer because the substrate and oxide layers had an overall thickness of 10.0 nm or greater. As such, higher pressures were very desirable to rapidly grow the first and second oxide layers to minimize production cycle time without sacrificing oxide uniformity and quality. In the present invention, however, such rapid growth is no longer desirable because the overall thickness of today's gate dielectrics has decreased to ultrathin size, i.e., less than about 7.5 nm. Furthermore, it has been surprisingly found that growing the oxide layer **12** under low pressure, typically 1.0 nm–2.5 nm, does not adversely affect the electrical or physical properties of the semiconductor. To the contrary, because of the low pressure grow-deposit-grow scheme provided by the present invention, the physical and electrical properties, as well as the overall quality, of the semiconductors manufactured in accordance with the present invention, are believed to be equal to those manufactured under the conventional stacked oxide synthesis discussed in the incorporated '370 patent. Furthermore, ultrathin, uniform oxide layers are now possible in a single furnace cluster step as provided by the present invention.

Under conventional processes, the oxide layer grows rapidly, making it extremely difficult to achieve a uniform, high quality, ultrathin gate dielectric that has an overall thickness of less than about 7.5 nm. Moreover, the conventional grow-deposit-grow processes were conducted in three different furnaces; two furnaces in which the pressure was kept at atmospheric pressure or greater to grow the thicker oxides and a third in which the pressure was sub-atmospheric to deposit the dielectric. In application of this conventional grow-deposit-grow process, the semiconductor was first placed in an atmospheric furnace, then transferred to a low pressure furnace and then transferred back to an atmospheric furnace. As well imagined, this three separate furnace operation increased cycle time and reduced throughput, which increased the overall cost of the semiconductor device.

In contrast, however, the present invention provides a process that allows the oxide layer **12** to be formed in a controlled manner to thicknesses well below the 3.0 nm required by today's sub-micron (e.g., 0.25 micrometer) technologies, which are particularly useful in CMOS and BiCMOS technologies and their enhancement modules. While, the controlled growth is somewhat dependent on the pressures at which the oxide is formed, flow concentration and growth temperatures also play a part in the oxide growth. Furthermore, the grow-deposit-grow scheme of the present invention can be conducted in a single low pressure cluster furnace, since the oxide layer **12** can be formed under the same low pressure environment under which a dielectric layer is deposited. The controlled growth of the oxide layer **12** provides a gate dielectric having an ultrathin, yet high quality and very uniform thickness, which is highly desirable in ultrathin stacked oxide gate formation.

Also, shown in FIG. 1 is the dielectric layer **14** formed over the oxide layer **12**. This dielectric layer **14** layer preferably contains a substantial concentration of a hydrogen isotope, such as deuterium. In addition, the dielectric layer **14** is preferably an oxygen permeable film that is transparent to O_2 species, and more preferably is silicon oxide (SiO_2). It is believed that the hydrogen isotope-containing dielectric layer of the present invention offers

further advantages that cooperate with the above-discussed advantages to provide a semiconductor device that has improved structural properties and also improved electrical properties. It is believed that the hydrogen isotope, which is incorporated into the dielectric layer **14** provides for a slower, and thus, more controlled deposition of the dielectric layer **14**. It is speculated that the slower deposition rate is due to the larger mass of the hydrogen isotope as opposed to the lesser mass nonisotopic hydrogen. It is further suggested that this slower deposition rate produces a more uniform layer that has fewer structural defects than dielectric layers that are formed with nonisotopic hydrogen. As such, then the uniformity would provide further stress-reducing interfaces within the semiconductor device, more specifically between the oxide layer **12** and the dielectric layer **14**. Furthermore, studies have indicated that when dielectrics are passivated with hydrogen isotopes, such as deuterium, there is less electrical degradation within the device, thereby enhancing the electrical properties of the semiconductor device as well. It is believed that the hydrogen isotope atoms are not as easily removed from the silicon atoms as is ordinary hydrogen. As such, fewer dangling bonds are formed over the same period of time, which can decrease the amount of degradation that occurs within the semiconductor device over a period of time.

In one advantageous embodiment, the dielectric layer **14** is deposited by the low pressure chemical vapor deposition decomposition of deuterated tetraethyl orthosilicate $Si(OC_2D_5)_4$ (or deuterated "TEOS") or the oxidation of deuterated silane SiD_4 in the presence of oxygen or nitrous oxide (N_2O). While these two gases have specifically been mentioned, it should be understood that other hydrogen isotope mixtures of gases, such as SiD_4, CO_2 and D_2, $SiCl_2H_2$ and N_2O, SiD_4 and N_2O, SiD_4 and NO, $Si(OC_2H_5)_4$ ("TEOS") a SiD_4 and O_2 or mixtures of any these gases. In a more advantageous embodiment, however, the gas mixture includes SiD_4 and D_2 and is added into the dielectric layer **14** during its deposition. Preferably, the gas includes less than 1 ppm of the nonisotopic hydrogen. The flow rate of the gaseous material will depend on the equipment used for depositions. These conditions combine to form a preferred deposition rate of the dielectric layer **14** of that may range from about 0.01 nm to about 10.0 nm per minute. The interface between layers **12** and **14** is shown by the horizontal line **16**. The deposition temperatures for the dielectric layer **14** may be in the same range as those stated above for the first grown oxide layer **12**. An exemplary pressure under which the dielectric layer **14** is deposited is about 400 milliTorr.

For reasons that are discussed below, not all combinations of dielectric materials are useful because the deposited dielectric **14** must have different defect structures from layer **12** to form the interface **16** and also **14** must be transparent to oxidizing species to anneal out the traps during the second growing step. For example, although the well-known SiO_2—Si_3N_4 structure has a low defect density, it also has a high density of traps that cannot be reduced by annealing. This structure is, therefore, not useful in the present invention, unless the nitride layer is completely consumed to form silicon oxynitride to make the layer semitransparent to oxidizing species. However, the thermally grown/deposited oxide structure of the present invention provides a low defect density as well as a deposited layer **14** that is transparent to an ambient oxidant and therefore, traps can be removed by annealing.

Continuing to refer to FIG. **1**, there is also illustrated a second grown oxide layer **18** formed between the substrate **10** and the oxide layer **12** during the third-step of synthesis. In preferred embodiments, this third oxide layer **18** is also thermally grown. The manufacturing temperature used to grow the oxide layer **12** and deposit the dielectric layer **14** is increased from about 650°C. to between about 800° C.–1000° C. These temperatures provide a densification/annealing oxidizing step, which, as the term suggests, both densities the existing oxide and deposited oxide dielectric layer **14**. In addition, the new oxide layer **18** is grown under stress-modulated conditions provided by the interface **16**, resulting in a planar and stress-free substrate/oxide **18** interface that is critical to device performance and reliability. In an advantageous embodiment, this anneal is conducted at a temperature that may range from about 800° C. to about 1000° C. and a pressure that may range from about 0.4 Torr to about 10 Torr, with a preferred pressure during this phase being 900 milliTorr. More preferably, the temperature is held at about 850° C. for approximately one hour. The growing oxidizing environment is a mixture of oxygen and nitrogen or nitrous oxide and nitrogen. The oxygen or nitrous oxide may have flow rates that range from about 0.5 slm to about 25 slm. In an exemplary embodiment, this procedure produces an oxide layer with a thickness ranging from about 0.5 nm to about 0.8 nm. The thermally grown second grown oxide layer **18** forms a planar and stress-free interface between the substrate **10** and the oxide layer **18** as it is grown under controlled stress modulation provided by the stress-accommodating interface **16** layer. The planar substrate/dielectric interface has desirable interfacial and electrical properties. Furthermore, the formation of the second grown oxide layer **18** provides a deuterated Si/SiO_2 interface with minimum roughness and stress gradient, both of which are highly desirable in sub-micron technologies for device performance and reliability.

During annealing, oxide growth occurs as the oxidizing species diffuses through the existing oxide and then reacts with silicon at the Si/SiO_2 interface. It has been found that the presence of a defect within the oxides enhances the transport of the oxidant by diffusion; that is, the defects provide paths for the oxidant. The newly grown SiO_2 is structurally superior to any other oxides because the growth occurs under the stress accommodating conditions provided by the interface **16**, which acts as a stress cushion. The interface **16** also acts as a defect sink and a barrier for the diffusional transport of ambient environmental contaminant ions to the Si/SiO_2 interface. The oxidation reactions during the densification anneal third step produces a reduction in the number of interface traps together with a simultaneous reduction in the Si/SiO_2 interface stress gradient, and roughness.

In contrast, in a conventional Si_3N_4/SiO_2 structure Si_3N_4 is opaque to the diffusion of the oxidant. During the oxidizing anneal, the top of the Si_3N_4 oxidizes to form silicon oxynitride without any oxidant transport to the interface. Thus, the density of interface states remains unchanged after an oxidizing anneal. Moreover, because the Si_3N_4 layer is relatively impervious to the diffusional transport of the oxidizing species, there is very little reduction in the interfacial roughness and number of asperities as there is no interfacial oxidation reaction during the densification anneal.

This concept of stacking can be achieved through variations of the composition of the materials that form the oxidized dielectric layers and the way in which they are formed. For example, onto the grown deuterated SiO_2 layer, a polysilicon layer may be deposited and oxidized or a thin nitride layer may be completely oxidized to deposit layer **14**. Other variations will be readily apparent by those skilled in the art.

As illustrated in FIG. 1, each layer has a plurality of defects, i.e., first grown and second deposited SiO_2 layers have different defect structures, which are schematically represented by the substantially vertical wavy lines. The defects are misaligned with respect to each other, that is, the defects within each layer terminate at the interface of grown oxide layer 12 and deposited dielectric layer 14. Defects for amorphous SiO_2 structures may be micropores, sudden change of local order, boundaries, etc. As understood from the incorporated '370 patent, misaligning defects across the interface reduces the defect density (D_o). For thin oxide gate dielectrics, the major contributors to D_o are the growth induced defect density and the intrinsic stress within the oxide layer. Defects form at energetically favored sites such as heterogeneities formed by localized contaminants, ion damaged areas and faulting on a silicon nucleation surface because of retarded oxidation. The-defects grow outward as oxidation consumes silicon around the defect and eventually a network of defects exists. The defects may be viewed as pipes for diffusional mass transport as well as potential current paths, which would have substantial impact on device performance and reliability. The misalignment of these defects, which is a direct result of the low pressure grow-deposit-grow scheme, greatly reduces the D_o, and thereby provides a high quality gate oxide.

With respect to density defects, it is known that stress incorporation in SiO_2 films is due to incomplete relaxation of the viscoelastic compressive stress at oxidation temperatures less than 900° C., and the thermal expansion mismatch between SiO_2 and Si. Moreover, complex device geometry and processing frequently result in locally high stress levels that induce the generation and propagation of defects thereby increasing both the size and density of defects. The interface made between two different dielectrics, such as two types of oxides, e.g., the thermally grown oxide layer 12 and the layer 14 and deposited oxide described with respect to FIG. 1. The interface effectively reduces the defect density by providing a discontinuity in the defect structure. The interface is not effective in reducing the effective defect density if the defects in the two dielectrics are aligned, i.e., if they are not misaligned and there is no discontinuity. Thus, it is highly advantageous that the defects are misaligned as in the present invention.

Turning now to FIG. 2, an advantageous embodiment of the generalized thermal schedule and gas flow sequence of the formation of the oxide layers will now be described, keeping in mind that exemplary broader ranges have been previously discussed. Time is plotted horizontally and temperature is plotted vertically. Both scales are in arbitrary units. The oxidation cycle begins with the growth of the first oxide layer 12 at t_1 with the insertion of the pre-gate cleaned silicon wafers under an atmosphere of O_2 at a temperature of about 650° C. into a low pressure furnace. The O_2 is preferably flowed over the silicon substrate at a rate that ranges from about 5 slm to about 25 slm. In a more advantageous embodiment, the flow rate is 9 slm. The pressure is maintained at 900 milliTorr, and the semiconductor (Si) is left under these conditions for about 1 hour to grow an oxide layer having a thickness of about 0.5–2.0 nm. At time t_2, the dielectric layer 14 is then formed by discontinuing the flow of O_2 and commencing a flow of N_2O at the rate of 1.75 slm and a flow of N_2 at the rate of 0.75 slm. The temperature is maintained at 650° C., but the pressure is dropped to about 400 milliTorr. Deuterated TEOS is introduced into the furnace at the rate of 50 cubic centimeters per minute (cc/min.). The semiconductor is left under these conditions for 0.5 hours to deposit a SiO_2 layer with a thickness of about 1.5 nm. At time t_3, the densification/annealing oxidizing step is then performed to density the composite oxide (layers 12 and 14) and to oxidize the substrate 10 and grow the second grown oxide layer 18. To accomplish this step, the temperature is increased to about 850° C., the flow of N_2 is discontinued and a flow of either a flow of O_2 or N_2O is commenced at a rate of 9 slm under a pressure of 900 milliTorr. This step is continued for about one hour to grow the second grown oxide layer 18 to a thickness of about 0.5 nm to about 0.8 nm. During this step, three events occur: (1) densification of layer 14, (2) removal of interface traps from the interface 16 between layers 12 and 14 and (3) growth of a stress-free oxide layer 18 that generates a planar Si/SiO_2 interface. Following this phase of the procedure, the semiconductor is removed from the low pressure furnace at time t_4. The deposited layer can also be achieved by low pressure oxidation of SiD_4 instead of deuterated TEOS.

From the foregoing, it is readily apparent that the present invention provides a gate dielectric and method of the manufacturer therefore that includes the steps of: (1) growing a first oxide layer on the semiconductor substrate in a zone of low pressure; (2) depositing a deuterated dielectric layer on the first oxide layer in the zone of low pressure; and (3) growing a second oxide layer between the first oxide layer and the substrate in the zone of low pressure. The zone of low pressure is created to retard oxidation rates so that ultrathin stacked oxide with high quality and robustness can be achieved.

The present invention therefore introduces the broad concept of low pressure stacked (grow-deposit-grow) oxide synthesis in a single thermal schedule. Such retardation of the growth rate is necessary, given the thinness and uniformity desired in the oxide sub-layers for sub-micron technologies. The resulting ultrathin stacked, SiO_2 structure has superior electrical and substructural properties over the conventional oxidation scheme of the prior art. This novel synthesis is achieved through the low pressure growing-depositing-growing of SiO_2 layers on silicon substrates by thermal oxidation, deuterated low pressure chemical vapor deposition ("LPCVD"), and densification/oxidation, respectively. The resulting stacked oxides have ultra-low defect density with excellent breakdown and interfacial characteristics.

Such low defect density in sub-micron technologies is comparable to that previously believed possible only for dual-dielectric Si_3N_4—SiO_2 interfaces. Moreover, it is believed that these stacked oxides of the present invention should have better robustness to severe ULSI processing. This improved robustness is due to resistant to hot-carrier aging, mobility degradation, with the added advantages due to deuterium incorporation in the stacked dielectric, in addition to the other superior physical and electrical properties as found in the stacked oxide semiconductors provided in the incorporated '307 patent.

Based on the studies conducted and disclosed in the '307 patent, the lowering in defect density, which is an aspect of the present invention, results from misaligning the micropores and other interconnecting defects within the stacked oxide layer and from annihilation of defects during densification/oxidation by the defect sink provided by the interface between the thermally grown and LPCVD-deposited SiO_2 layers. The superior Si—SiO_2 interfacial characteristics of the stacked oxide are due to the excellent substructure of the SiO_2 grown during low pressure densification/oxidation annealing in near-equilibrium conditions in the presence of a stress-accommodating interface

Furthermore, there are other additional advantages, as explained above, associated with the deuterating the deposited oxide layer.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

What is claimed is:

1. A semiconductor wafer having a gate dielectric located thereon and having a thickness of less than about 7.5 nm, comprising:

a first grown oxide layer having a thickness ranging from about 1 nm to less than about 5 nm and located on a substrate of said semiconductor wafer and having been formed on an exposed surface of said substrate in a zone of low pressure ranging from about 0.2 millitorr to about 10 millitorr;

a deposited oxide dielectric layer having a substantial concentration of hydrogen isotope incorporated therein wherein a concentration of said hydrogen isotope is at least about 10^{16} cm^{-3}; said dielectric layer formed over said first oxide layer in said zone of low pressure

a stress-accommodating interface located between said first grown oxide layer and said deposited oxide dielectric layer; and

a second grown oxide layer located between said substrate and said first grown oxide layer, said stress-accommodating interface located between said first oxide layer and said substrate, said second oxide layer formed in said zone of low pressure.

2. The semiconductor wafer as recited in claim 1 wherein said second grown oxide layer has a thickness of less than 1 nm.

3. The semiconductor wafer as recited in claim 2 wherein said thickness is about 3.0 nm.

4. The semiconductor wafer as recited in claim 1 wherein said deposited oxide dielectric layer comprises an oxidized deuterated tetraethyl orthosilicate (TEOS) and has a thickness of about 1.5 nm.

5. The semiconductor wafer as recited in claim 1 wherein a thickness of said second grown oxide layer ranges from about 1 nm to about 4.0 nm.

6. The semiconductor wafer as recited in claim 1 further including nitrogen ranging in concentration of from about 1% to about 5% near said stress-accommodating interface.

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United States Patent [19]

Brady et al.

[11] Patent Number: 5,940,736

[45] Date of Patent: Aug. 17, 1999

[54] **METHOD FOR FORMING A HIGH QUALITY ULTRATHIN GATE OXIDE LAYER**

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[73] Assignee: **Lucent Technologies Inc.**, Murray Hill, N.J.

[21] Appl. No.: **08/814,670**

[22] Filed: **Mar. 11, 1997**

[51] **Int. Cl.**[6] **H01L 21/02**

[52] **U.S. Cl.** **438/787**; 438/787; 438/790; 438/770; 438/762

[58] **Field of Search** 438/787, 790, 438/770, 762

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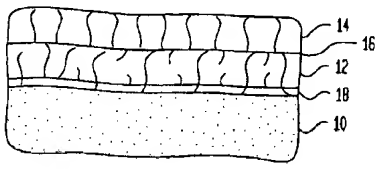
Primary Examiner—Charles Bowers
Assistant Examiner—Thanh Nguyen

[57] **ABSTRACT**

This invention includes a novel synthesis of a three-step process of growing, depositing and growing SiO_2 under low pressure, e.g., 0.2–10 Torr, to generate high quality, robust and reliable gate oxides for sub 0.5 micron technologies. The first layer, 1.0–3.0 nm is thermally grown for passivation of the Si-semiconductor surface. The second deposited layer 1.0–5.0 nm forms an interface to with the first grown layer. During the third step of the synthesis densification of the deposited oxide layers occurs with a simultaneous removal of the interface traps at the interface and growth of a stress-modulated SiO_2 occurs at the Si/first grown layer interface in the presence of a stress-accommodating interface layer resulting in a planar and stress-reduced Si/SiO_2 interface. The entire synthesis is done under low-pressure (e.g., 0.2–10 Torr) for slowing down the oxidation kinetics to achieve ultrathin sublayers and may be done in a single low-pressure furnace by clustering all three steps. For light nitrogen-incorporation (<5%) for certain devices, often required due to improved resistance to boron and other dopant diffusion and hot-carrier characteristics, N_2O or NO in the oxidant are used during each steps of the stacked oxide synthesis. Planar and stress-reduced Si/SiO_2 interface characteristics is a unique signature of stacked oxide that improves robustness of the gate oxide to ULSI processing resulting in reduced scatter in device parameters (e.g., threshold voltage transconductance), mobility degradation and resistance to hot-carrier and Fowler-Nordheim stress.

13 Claims, 1 Drawing Sheet



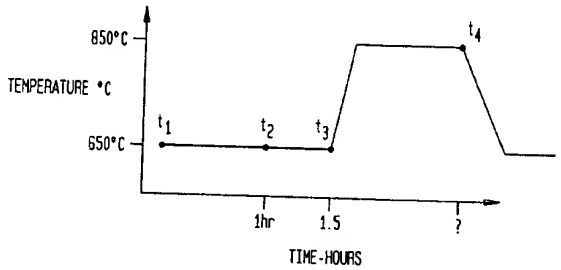


FIG. 1

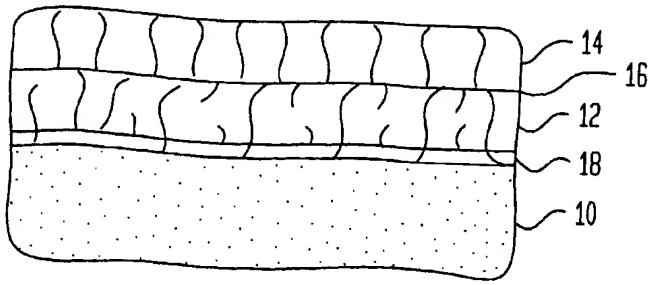

14
16
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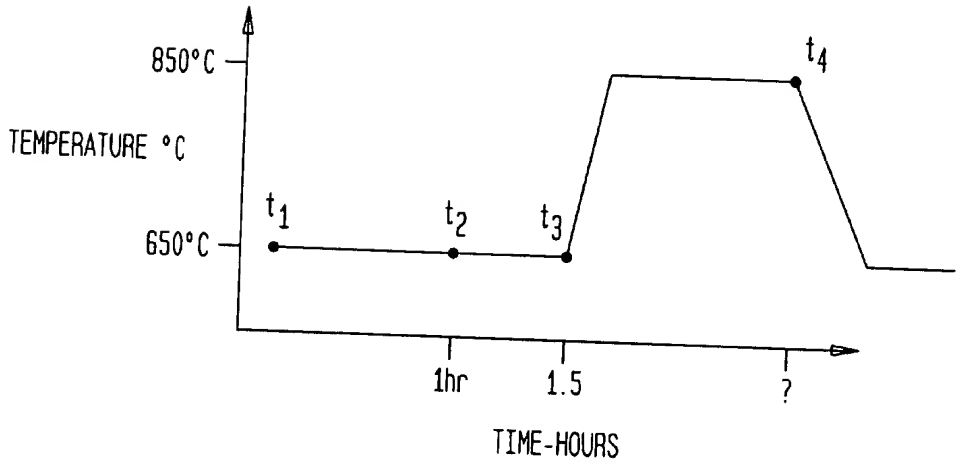
FIG. 2


850°C
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METHOD FOR FORMING A HIGH QUALITY ULTRATHIN GATE OXIDE LAYER

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to integrated circuit fabrication and, more specifically, to a system and method for forming a uniform, ultrathin gate oxide layer on a semiconductor substrate.

BACKGROUND OF THE INVENTION

As metal-oxide-semiconductor ("MOS") technology continues to advance and the features of the MOS devices shrink, a scaling down in the vertical dimension of the devices typically occurs. Critical to the success of these devices is a reliable, high-quality gate dielectric with a low defect density ("D_o") and a high breakdown field strength ("F_{bd}") that retains its quality during advanced processing. As the overall size of the semiconductors get ultrathin (e.g., less than 7.5 nm), the quality of the oxide (e.g., SiO_2), even under the best possible external growth conditions, is limited by the natural viscoelastic compressive stress generated in the SiO_2 at temperatures below 1000° C. and by the thermal expansion mismatch between silicon substrate and SiO_2. In present applications, a genuine lowering of the D_o in the range of 0.05 to 0.5 cm^{-2} has been achieved. For example, oxide/nitride or oxide/nitride/oxide (ONO) structures can attain such low D_o. The Si_3N_4—SiO_2 ("silicon nitride-silicon oxide") interface, however, is invariably associated with a high density of interface states ("Q_{it}") that cannot be annealed out easily because the Si_3N_4 layer is impervious to diffusion of oxidizing species. These multi-layered dielectrics are unsuitable as gate dielectrics in advanced complementary metal-oxide-semiconductor ("CMOS") integrated circuits, because the interface states can cause charge-induced shift in the threshold voltage and can reduce the channel conductance during operation.

To overcome this problem, the concept of stacking thermally grown and chemical-vapor-deposited ("CVD") SiO_2 structures has been proposed in U.S. Pat. No. 4,851,370 ("the '370 patent"), which is incorporated herein by reference for all purposes. Here, the composite stack is synthesized by a 3-step grow-deposit-grow technique wherein the growing steps are conducted at pressures equal to or greater than one atmosphere. The interface between the grown and deposited SiO_2 layers serves the same purpose as the interface in SiO_2—Si_3N_4 structures (i.e., it reduces the D_o by misaligning the defects across the interface). Moreover, the interface traps in stacked oxide structures that can be removed easily by an oxidizing anneal, since the top deposited SiO_2 layer, unlike the Si_3N_4 film, is transparent to oxidizing species (i.e., it transports them by diffusion). This stacking concept can be applied to any composite dielectric structure with similar results as long as the top deposited dielectric layer is transparent to the oxidizing species.

A few major factors contributing to defects in conventional thin-oxide gate dielectrics are growth-induced micropores and intrinsic stress within the oxide layer. The micropores are 1.0 nm to 2.5 nm in diameter, with an average separation of about 10.0 nm. The pores form at energetically favored sites such as heterogeneities created by localized contaminants, ion-damaged areas, dislocation pile-ups and other defect areas on the silicon surface resulting from retarded oxidation in these sites. The pores grow outward as oxidation continues to consume silicon around the pore. Thus, a network of micropores usually exists in SiO_2. The micropore network forms potential short-circuit paths for diffusional mass transport and for current leakage.

In addition, the stress within a SiO_2 layer, often accentuated by complex device geometries and processing, usually increases both the size and density of the micropores. Therefore, in developing thin dielectrics with ultra-low D_o, not only should the initial D_o be reduced, but also the local stress-gradients near the Si—SiO_2 interface should be reduced by providing a stress-accommodating layer, such as an interface (between grown and deposited layers) within the dielectric that acts as a stress cushion and defect sink.

The above-mentioned problems become even more acute as the overall size of devices decrease to sub-micron size with ultrathin gate dielectrics (e.g., less than 7.5 nm). Unfortunately, however, the above-discussed conventional stacked-oxide process, which works extremely well in technologies where the semiconductor thickness is greater than 7.5 nm, is not as applicable in technologies having thicknesses less than 7.5 nm. The main reason for this is that in the conventional 3-step stacked process, the SiO_2 is grown in pressures of one atmosphere or greater. In semiconductor technologies where the gate oxide thickness is 10.0 nm or greater, this particular condition is most advantageous because under such atmospheric pressure, the SiO_2 can be grown quite rapidly and one can grow the first grown layer (typically 3.5–7.5 nm) with good uniformity. This rapid growth is highly desirable, for it cuts down in manufacturing time, and thus, overall production costs. This same rapid growth, which is so advantageous in technologies with gate oxide thickness of **10.0** nm or greater is less desirable in sub-0.5 micron semiconductor technologies because the oxides grow too quickly, which makes thicknesses harder to control. As such, the oxide layers are less uniform in thickness, which is unacceptable.

Accordingly, what is needed in the art is a stacked-oxide process that provides semiconductors having thicknesses of less than 10.0 nm and, more advantageously less than 7.5 nm, and yet provides a semiconductor that has a low defect density ("D_o") and a high breakdown field strength ("F_{bd}") that retains its quality during advanced processing. The present invention addresses this need.

SUMMARY OF THE INVENTION

To address the above-discussed deficiencies of the prior art, the present invention provides a semiconductor and systems and methods of manufacture thereof. One method includes the following grow-deposit-grow steps: (1) growing a first oxide layer on the semiconductor substrate in a zone of low pressure, (2) depositing a dielectric layer on the first oxide layer in the zone of low pressure and (3) growing a second oxide layer between the first oxide layer and the substrate in the zone of low pressure. The zone of low pressure is created to retard the oxidation rate at which the first and second oxide layers are grown.

The present invention therefore introduces the broad concept of growing the first and second oxide layers under low pressure oxidizing conditions to retard their growth. Such retardation of the growth rate is necessary given the thinness and uniformity desired in the dielectric sub-layers in sub-micron technologies.

In one embodiment of the present invention, the second grown oxide layer may have a thickness of less than 10 nm or between about 0.5 nm and about 0.8 nm and may be grown at a temperature exceeding 800° C.

In one embodiment of the present invention, the steps of growing, depositing and growing are performed in a single vapor deposition equipment. That the method of the present invention may be performed in a single "tool" or "furnace"

allows high rates of production and greater process control, although, performance in a single tool is not required.

In one embodiment of the present invention, a pressure in the zone of low pressure ranges from about 200 milliTorr to about 950 milliTorr. In a more specific embodiment, the pressure is about 900 milliTorr during the step of growing the first and second oxide layers and about 400 milliTorr during the second step of depositing the dielectric layer.

In one embodiment of the present invention, a thickness of the first grown oxide layer is less than about 5.0 nm. In a more specific embodiment of the present invention, however, the thickness is about 3.0 nm.

In another embodiment of the present invention, the deposited dielectric layer is generated from the decomposition of tetraethyl orthosilicate ("TEOS") and has a thickness of about 1.5 nm. In a more specific embodiment of the present invention, the thickness ranges from about 1 nm to about 4.0 nm. The TEOS is preferably deposited at a flow rate of 50 cubic centimeters per minute.

In one embodiment of the present invention, the steps of growing and depositing are performed at a temperature that ranges from about 600° C. to about 750° C. In yet another embodiment, the step of growing the second oxide layer is performed at a temperature ranging from about 800° C. to about 1000° C.

In one embodiment of the present invention, the step of growing the first oxide layer is performed under a pressure of 900 milliTorr and the oxygen has a flow rate of 9 standard liters per minute. In yet another embodiment, the step of growing is performed under a nitrous oxide and nitrogen environment wherein the nitrous oxide has a flow rate of about 1.72 standard liters per minute and the nitrogen has a flow rate of about 0.75 standard liters per minute to attain light-nitridation, (1–5%) near the interface between the first and second grown oxide layers.

In another aspect of the present invention, a semiconductor comprised of a substrate and having a stress-accommodating layer formed therein is provided. The semiconductor has a thickness less than 7.5 nm and comprises: (1) a first grown oxide layer on the substrate that was formed on an exposed surface of the substrate in a zone of low pressure, (2) a deposited dielectric layer on the first grown oxide layer that was formed over the first grown oxide layer in the zone of low pressure and (3) a second grown oxide layer formed between the first oxide layer and the substrate that was formed in the zone of low pressure. The zone of low pressure is created to retard a rate at which the first and second oxide layers are grown. During this third-step of stacked oxide synthesis oxide growth occurs under a stress-modulating condition provided by the interface between the first grown and second deposited layer generating a planar and stress-free substrate Si/SiO_2 interface which can otherwise never be achieved by conventional 1-step oxide growth.

In one embodiment of this aspect of the present invention, the first grown oxide, the second deposited dielectric and the second grown oxide layers are formed on the substrate in a single low-pressure vapor deposition equipment. As previously stated, this offers the advantage of decrease production cycle time and thus production cost.

In one embodiment of this aspect of the present invention, the second grown oxide layer may be formed at a temperature exceeding about 800° C., and the first oxide layer and the dielectric layer may be grown in a temperature exceeding about 600° C. The second grown oxide layer may have thickness that ranges from about 0.5 nm to about 0.8 nm.

In one embodiment of this aspect of the present invention, the deposited dielectric layer is formed in a pressure of about 400 milliTorr in the zone of low pressure and may have a thickness of about 10.5 nm. In yet another aspect of this particular embodiment, the deposited dielectric layer is formed from the decomposition of TEOS, which preferably had a flow rate of 50 cubic centimeters per minute during its deposition.

In one embodiment of this aspect of the present invention, the first oxide layer may have a thickness of less than about 5.0 nm (preferably in the range of 1.0 nm to 3.0 nm).

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates a schematic representation of a structure according to an advantageous embodiment of the present invention; and

FIG. 2 illustrates a schematic graph of the thermal, pressure and flow rate history for an oxidation scheme in accordance with an advantageous embodiment of the present invention.

DETAILED DESCRIPTION

Referring initially to FIG. 1, there is illustrated a schematic representation of a structure according to an advantageous embodiment of the present invention. In one such embodiment, a substrate **10** is used, and a 1 nm to 2.5 nm oxide layer **12** is formed on the substrate under a low pressure, for example, a pressure of less than 10 Torr. In more advantageous embodiments, the pressures are at less than about 2 Torr. In one advantageous embodiment, the substrate **10** may be silicon and the oxide layer **12** may be silicon dioxide (SiO_2) that is thermally grown from the substrate **10** to a thickness that may range from about 1 nm to about 2.5 nm. However, it will be appreciated by those skilled in the art that other materials presently used in the manufacturer of semiconductor devices may be used or materials later-determined to be useful for such manufacture may also be used. Moreover, it is within the scope of the present invention that the oxide layer **12** could also be deposited, as long as it has a different defect structure compared to the second deposited layer. However, as just mentioned above, it is desirable that the oxide layer **12** be thermally grown. Depending on the particular embodiment, the low pressure under which the oxide layer **12** is grown may range from about 0.4 Torr to about 10 Torr and the temperature may range from about 350° C. to about 1000° C. In one embodiment, the oxygen flow may be at a rate that ranges from about 5 standard liters per minute (slm) to about 25 slm. However, in an advantageous embodiment, the pressure under which the oxide layer **12** is grown under a

pressure of about 900 milliTorr and the temperature may range from about 600° C. to about 750° C.

Forming the oxide layer **12** under low pressure is a radical departure from the conventional stacked oxide synthesis, in which the oxide layer is grown under a pressure of one atmosphere or greater. In conventional stacked oxides, pressures of one atmosphere or greater were necessary to grow the first oxide layer because the substrate and oxide layers had an overall thickness of 10.0 nm or greater. As such, higher pressures were very desirable to rapidly grow the first and second oxide layers to minimize production cycle time without sacrificing oxide uniformity and quality. In the present invention, however, such rapid growth is no longer desirable because the overall thickness of today's semiconductors has decreased to ultrathin size, i.e., less than about 7.5 nm. Furthermore, it has been surprisingly found that growing the oxide layer **12** under low pressure, typically 1.0 nm–2.5 nm, does not adversely affect the electrical or physical properties of the semiconductor. To the contrary, because of the low pressure grow-deposit-grow scheme provided by the present invention, the physical and electrical properties, as well as the overall quality, of the semiconductors manufactured in accordance with the present invention, are believed to be equal to those manufactured under the conventional stacked oxide synthesis discussed in the incorporated '370 patent. Furthermore, ultrathin, uniform oxide layers are now possible in a single furnace cluster step as provided by the present invention.

Under conventional processes, the oxide layer grows rapidly, making it extremely difficult to achieve a uniform, high quality, ultrathin semiconductor that has an overall thickness of less than about 7.5 nm. Moreover, the conventional grow-deposit-grow process were conducted in three different furnaces; two furnaces in which the pressure was kept at atmospheric pressure or greater to grow the thicker oxides and a third in which the pressure was subatmospheric to deposit the dielectric. In application of this conventional grow-deposit-grow process, the semiconductor was first placed in an atmospheric furnace, then transferred to a low pressure furnace and then transferred back to an atmospheric furnace. As well imagined, this three separate furnace operation increased cycle time and reduced throughput, which increased the overall cost of the semiconductor device.

In contrast, however, the present invention provides a process that allows the oxide layer **12** to be formed in a controlled manner to thicknesses well below the 3.0 nm required by today's sub-micron (e.g., 0.25 microns) technologies, which are particularly useful in CMOS and BiCMOS technologies and their enhancement modules. While, the controlled growth is somewhat dependent on the pressures at which the oxide is formed, flow concentration and growth temperatures also play a part in the oxide growth. Furthermore, the grow-deposit-grow scheme of the present invention can be conducted in a single low pressure cluster furnace since the oxide layer **12** can be formed under the same low pressure environment under which a dielectric layer is deposited. The controlled growth of the oxide layer **12** provides a semiconductor having a ultrathin, yet high quality and very uniform thickness, which is highly desirable in ultrathin stacked oxide gate formation.

Also shown in FIG. 1 is the dielectric layer **14** formed over the oxide layer **12**. This deposited oxide layer is, preferably an oxygen permeable film that is transparent to O_2 species, and more preferably is silicon oxide (SiO_2). In one advantageous embodiment, the dielectric layer **14** is deposited by the low pressure chemical vapor deposition decomposition of tetraethyl orthosilicate ("TEOS") or the oxidation of silane SiH_4 in the presence of oxygen or nitrous oxide (N_2O) . The flow rate of material, which may be TEOS, may range from about 10 to about 100 cc/min, with the flow rate of the O_2 or the N_2O ranging from about 0.5 slm to about 5 slm. These conditions combine to form a preferred deposition rate of the dielectric layer that may range from about 0.01 nm to about 10.0 nm per minute. The interface between these layers **12** and **14** is shown by the horizontal line **16**. The deposition temperatures for the dielectric layer **14** may be in the same range as those stated above for the first grown oxide layer **12**. An exemplary pressure under which the dielectric layer **14** is deposited is about 400 milliTorr.

For reasons that are discussed below, not all combinations of dielectric materials are useful because the deposited dielectric **14** must have different defect structures from layer **12** to form the interface **16** and also **14** must be transparent to oxidizing species to anneal out the traps during the second growing step. For example, although the well known SiO_2—Si_3N_4 structure has a low defect density, it also has a high density of traps that cannot be reduced by annealing. This structure is, therefore, not useful in the present invention, unless the nitride layer is completely consumed to form silicon oxynitride to make the layer semitransparent to oxidizing species. However, the thermally grown/deposited oxide structure of the present invention provides a low defect density as well as a deposited layer **14** that is transparent to oxidant ambient and therefore, traps can be removed by annealing.

Continuing to refer to FIG. 1, there is also illustrated a second grown oxide layer **18** formed between the substrate **10** and the oxide layer **12** during the third-step of synthesis. In preferred embodiments, this third oxide layer **18** is also thermally grown. The manufacturing temperature used to grow the oxide layer **12** and deposit the dielectric layer **14** is increased from about 650° C. to between about 800° C.–1000° C. These temperatures provide a densification/annealing oxidizing step, which, as the term suggests, both densifies the existing oxide and deposited oxide dielectric layer **14**. In addition, the new oxide layer **18** is grown under stress-modulated conditions provided by the interface **16**, resulting in a planar and stress-free substrate/oxide (**18**) interface that is critical to device performance and reliability. In an advantageous embodiment, this anneal is conducted at a temperature that may range from about 800° C. to about 1000° C. and a pressure that may range from about 0.4 Torr to about 10 Torr, with a preferred pressure during this phase being 900 milliTorr. More preferably, the temperature is held at about 850° C. for approximately one hour. The growing oxidizing environment is a mixture of oxygen and nitrogen or nitrous oxide and nitrogen. The oxygen or nitrous oxide may have flow rates that range from about 0.5 slm to about 25 slm. In an exemplary embodiment, this procedure produces an oxide layer with a thickness ranging from about 0.5 nm to about 0.8 nm. The thermally grown second grown oxide layer **18** forms a planar and stress-free interface between the substrate **10** and the oxide layer **18** as it is grown under controlled stress modulation provided by the stress-accommodating interface **16** layer. The planar substrate/dielectric interface has desirable interfacial and electrical properties. Furthermore, the formation of the second grown oxide layer **18** provides an Si/SiO_2 interface with minimum roughness and stress gradient, both of which are highly desirable in sub-micron technologies for device performance and reliability.

During annealing, oxide growth occurs as the oxidizing species diffuses through the existing oxide and then reacts

with silicon at the Si/SiO_2 interface. It has been found that the presence of defect within the oxides enhances the transport of the oxidant by diffusion; that is, the defects provide paths for the oxidant. The newly grown SiO_2 is structurally superior than any other oxides because the growth occurs under the stress accommodating conditions provided by the interface **16**, which acts as a stress cushion. The interface **16** also acts as a defect sink and as a barrier for the diffusional transport of contaminant ions from the ambient environment to the Si/SiO_2 interface. The oxidation reaction during the densification anneal third step produces a reduction in the number of interface traps together with a simultaneous reduction in the Si/SiO_2 interface stress gradient, and roughness.

In contrast, in a conventional Si_3N_4/SiO_2 structure Si_3N_4 is opaque to the diffusion of the oxidant. During the oxidizing anneal, the top of the Si_3N_4 oxidizes to form silicon oxynitride without any oxidant transport to the interface. Thus, the density of interface states remains unchanged after an oxidizing anneal. Moreover, because the Si_3N_4 layer is relatively impervious to the diffusional transport of the oxidizing species, there is very little reduction in the interfacial roughness and number of asperities as there is no interfacial oxidation reaction during the densification anneal.

This concept of stacking can be achieved through variations of the composition of the materials that form the oxidized dielectric layers and the way in which they are formed. For example, onto the grown SiO_2 layer a polysilicon layer may be deposited and oxidized or a thin nitride layer may be completely oxidized to deposit layer **14**. Other variations will be readily apparent by those skilled in the art.

As illustrated in FIG. 1, each layer has a plurality of defects, i.e. first grown and second deposited SiO_2 layers have different defect structures, which are schematically represented by the substantially vertical wavy lines. The defects are misaligned with respect to each other, that is, the defects within each layer terminate at the interface of grown oxide layer **12** and deposited dielectric layer **14**. Defects for amorphous SiO_2 structures may be micropores, sudden change of local order, boundaries, etc. As understood from the incorporated '370 patent, misaligning defects across the interface reduces the defect density (D_o) For thin oxide gate dielectrics, the major contributors to D_o are the growth induced defect density and the intrinsic stress within the oxide layer. Defects form at energetically favored sites such as heterogeneities formed by localized contaminants, ion damaged areas and faulting on silicon nucleation surface because of retarded oxidation. The defects grow outward as oxidation consumes silicon around the defect and eventually a network of defects exists. The defects may be viewed as pipes for diffusional mass transport as well as potential current paths, which would have substantial impact on device performance and reliability. The misalignment of these defects, which is a direct result of the low pressure grow-deposit-grow scheme, greatly reduces the D_o, and thereby provides a high quality gate oxide.

With respect to density defects, it is known that stress incorporation in SiO_2 films is due to incomplete relaxation of the viscoelastic compressive stress at oxidation temperatures less than 900° C., and the thermal expansion mismatch between SiO_2 and Si. Moreover, complex device geometry and processing frequently results in locally high stress level that induce the generation and propagation of defects thereby increasing both the size and density of defects. The interface made between two different dielectrics, such as two types of oxides, e.g., the thermally grown oxide layer **12** and the layer **14** and deposited oxide described with respect to FIG. **1**. The interface effectively reduces the defect density by providing a discontinuity in the defect structure. The interface is not effective in reducing the effective defect density if the defects in the two dielectrics are aligned, i.e., if they are not misaligned and there is no discontinuity. Thus, it is highly advantageous that the defects be misaligned as in the present invention.

Turning now to FIG. **2**, an advantageous embodiment of the generalized thermal schedule and gas flow sequence of the formation of the oxide layers will now be described, keeping in mind that exemplary broader ranges have been previously discussed. Time is plotted horizontally and temperature is plotted vertically. Both scales are in arbitrary units. The oxidation cycle begins with the growth of the first oxide layer **12** at t_1 with the insertion of the pre-gate cleaned silicon wafers under an atmosphere of O_2 at a temperature of about 650° C. into a low pressure furnace. The O_2 is preferably flowed over the silicon substrates at a rate that ranges from about 5 slm to about 25 slm. In a more advantageous embodiment, the flow rate is 9 slm. The pressure is maintained at 900 milliTorr, and the semiconductor (Si) is left under these conditions for about 1 hour to grow an oxide layer having a thickness of about 3.0 nm. At time t_2 The dielectric layer **14** is then formed by discontinuing the flow of O_2 and commencing a flow of N_2O at the rate of 1.75 slm and a flow of N_2 at the rate of 0.75 slm. The temperature is maintained at 650° C., but the pressure is dropped to about 400 milliTorr. TEOS is introduced into the furnace at the rate of 50 cubic centimeters per minute (cc/min.).

The semiconductor is left under these conditions for 0.5 hours to deposit a SiO_2 layer with a thickness of about 1.5 nm. At time t_3 The densification/annealing oxidizing step is then performed to densify the composite oxide (layers **12** and **14**) and to oxidize the substrate **10** and grow the second grown oxide layer **18**. To accomplish this step, the temperature is increased to about 850° C., the flow of N_2 is discontinued and either a flow of O_2 or N_2O is commenced at a rate of 9 slm under a pressure of 900 milliTorr. This step is continued for about one hour to grow the second grown oxide layer **18** to a thickness of about 0.5 nm to about 0.8 nm. During this step, three events occur: (1) densification of layer **14**, (2) removal of interface traps from the interface **16** between layers **12** and **14** and (3) growth of a stress-free oxide layer **18** that generates a planar Si/SiO_2 interface. Following this phase of the procedure, the semiconductor is removed from the low pressure furnace at time t_4.

From the foregoing, it is readily apparent that the present invention provides a semiconductor and method of manufacturer therefore that includes the steps of: (1) growing a first oxide layer on the semiconductor substrate in a zone of low pressure; (2) depositing a dielectric layer on the first oxide layer in the zone of low pressure; and (3) growing a second oxide layer between the first oxide layer and the substrate in the zone of low pressure. The zone of low pressure is created to retard oxidation rates so that ultrathin stacked oxide with high quality and robustness can be achieved.

The present invention therefore introduces the broad concept of low pressure stacked (grow-deposit-grow) oxide synthesis in a single thermal schedule. Such retardation of the growth rate is necessary, given the thinness and uniformity desired in the oxide sub-layers for sub-micron technologies. The resulting ultrathin stacked SiO_2 structure has superior electrical and substructural properties over the conventional oxidation scheme of the prior art. This novel

synthesis is achieved through the low pressure growing-depositing-growing of SiO_2 layers on silicon substrates by thermal oxidation, low pressure chemical vapor deposition ("LPCVD"), and densification/oxidation, respectively. The resulting stacked oxides have ultra-low defect density with excellent breakdown and interfacial characteristics.

Such low defect density in sub-micron technologies is comparable to that previously believed possible only for dual-dielectric Si_3N_4—SiO_2 interfaces. Moreover, it is believed that these stacked oxides of the present invention should have better robustness to severe ULSI processing, resistant to hot-carrier aging, mobility degradation, and narrow channel degradation behavior, in addition to the other superior physical and electrical properties as found in the stacked oxide semiconductors provided in the incorporated '307 patent.

Based on the stu dies conducted and disclosed in the '307 patent, the lowering in defect density, which is an aspect of the present invention, results from misaligning the micropores and other interconnecting defects within the stacked oxide layer and from annihilation of defects during densification/oxidation by the defect sink provided by the interface between the thermally grown and LPCVD-deposited SiO_2 layers. The superior Si—SiO_2 interfacial characteristics of the stacked oxide are due to the excellent substructure of the SiO_2 grown during low pressure densification/oxidation annealing in near-equilibrium conditions in the presence of a stress-accommodating interface layer.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

What is claimed is:

1. A method of forming an oxide layer on a semiconductor substrate, comprising:

growing a first oxide layer on said substrate in a zone of low pressure;

depositing a dielectric layer on said first oxide layer in said zone of low pressure; and

growing a second oxide layer between said first oxide layer and said substrate in said zone of low pressure, said zone of low pressure created to retard a rate at which said first and second oxide layers are grown thereby to provide a stress-accommodating layer within said semiconductor substrate, said growing, depositing and growing performed in a single vapor deposition device.

2. The method as recited in claim **1** wherein during said growing said first and second oxide layers a pressure in said zone of low pressure ranges from about 350 milliTorr to about 950 milliTorr.

3. The method as recited in claim **2** wherein said zone of low pressure is about 900 milliTorr during said growing said first and second oxide layers.

4. The method as recited in claim **1** wherein said zone of low pressure is about 400 milliTorr.

5. The method as recited in claim **1** wherein a thickness of said first oxide layer is less than about 5.0 nm.

6. The method as recited in claim **5** wherein said thickness is about 3.0 nm.

7. The method as recited in claim **1** wherein said dielectric layer is generated from the decomposition of tetraethyl orthosilicate (TEOS) and has a thickness of about 1.5 nm.

8. The method as recited in claim **7** wherein said TEOS has a flow rate of about 50 cubic centimeters per minute.

9. The method as recited in claim **1** wherein said second oxide layer has a thickness that ranges from about 1 nm to about 4.0 nm.

10. The method as recited in claim **1** wherein said growing and depositing are performed at a temperature that ranges from about 600° C. to about 750° C.

11. The method as recited in claim **1** wherein said growing said second oxide layer is performed at a temperature ranging from about 800° C. to about 1000° C.

12. The method as recited in claim **1** wherein said growing said first oxide layer is performed under a pressure of 900 milliTorr and oxygen having a flow rate of 9 standard liters per minute.

13. The method as recited in claim **1** wherein said depositing is performed under a nitrous oxide and nitrogen environment wherein said nitrous oxide has a flow rate of about 1.72 standard liters per minute and said nitrogen has a flow rate of about 0.75 standard liters per minute.

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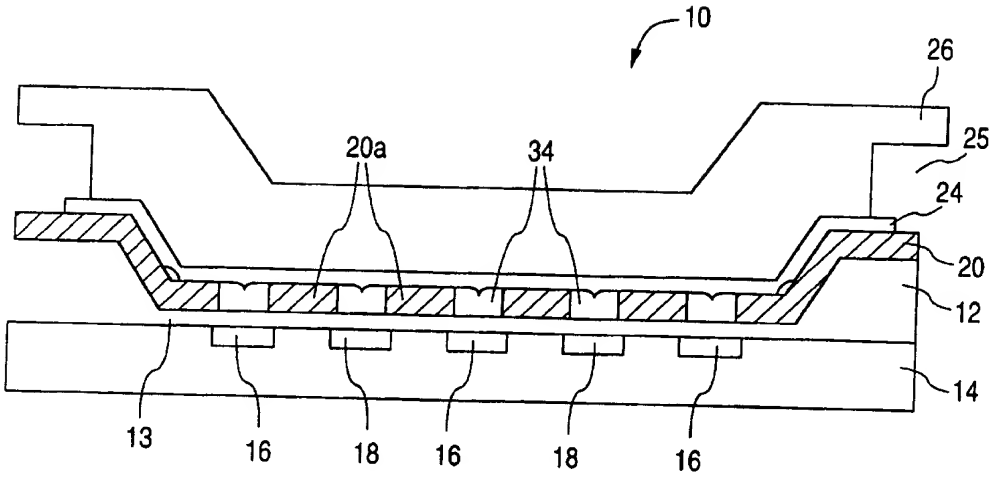

FIGURE 2

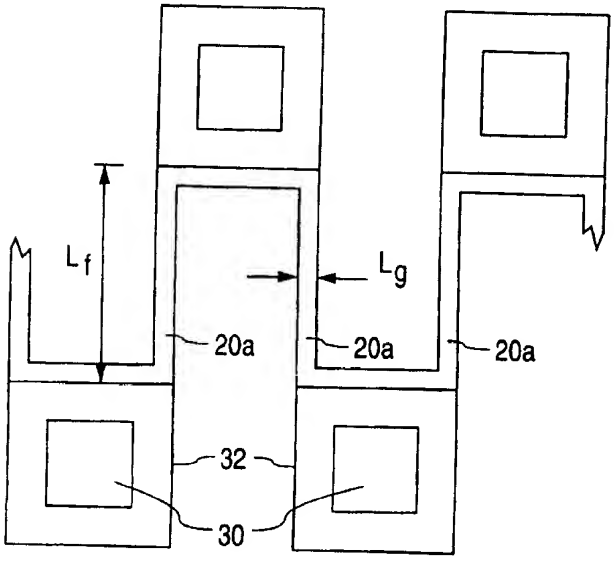

FIGURE 3